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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,928	08/04/2003	Soichi Kobayashi	009683-476	4942

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EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,928	KOBAYASHI ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *28 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4 and 6-9* is/are pending in the application.

4a) Of the above claim(s) *2 and 5* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 & 6-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 8/4/03 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/28/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered April 28, 2006.

- Claims 1-9 are pending.
- Claims 1, 3, & 4 are amended.
- Claims 2 & 5 are canceled.

Response to Amendment

1) Applicant's arguments, with respect to amended claims 1, 3, & 4 and previously presented claims 6-9 have been fully considered and are persuasive. The 102(b) rejection under Urakawa US Pat no. 6,324,106 B2 has been withdrawn.

2) Applicant's arguments and amendments with respect to amended claims 1, 3, & 4 and previously presented claims 6-9 filed April 28, 2006 have been fully considered but they are not persuasive. The 102(b) rejection over Kawamata and 103(a) rejection over Kawamata, further in view of Urakawa stands. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends, that Kawamata fails to teach or suggest a) a plurality of modules have word lines different in number or b) a control circuit, included in a module that does not have a maximum number of word lines, controls an operation in a test mode for reading or writing irrespective of a value of a chip select signal. The Examiner respectfully disagrees.

Kawamata teaches "the semiconductor memory shown in FIG. 1, in the memory cell array 200 there is accessed a memory cell designated by a word line selected by an X decoder 201, which receives and decodes an X address and selects a word line designated by the X address, and a digit line selected by a Y decoder 202, which receives and decodes a Y address and selects a digit line designated by the Y address." (Figure 1, paragraph [0004]). Kawamata adds, "Here, it is assumed that the address for selection of the redundant rows is composed of X0 to X4 (namely, 32 redundant word lines are provided)" (paragraph [0067]). Hence, clearly the invention in question does in fact teach modules with word lines.

Secondly Kawamata teaches "a control circuit writes fail information.."(abstract), and again in claims 3, 4, 6, & 9 "when said redundant cells in said semiconductor memory under test are tested; and control means for writing fail information into said redundant cell fail information memory at said redundant cell fail information memory address thus synthesized, when at least one of said comparison results outputted in parallel from said plurality of comparators indicates a "fail"." Hence, clearly Kawamata teaches a control circuit that writes information during the test mode.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-4, & 6 are rejected under 35 U.S.C. 102(b) as being fully anticipated by Kawamata US PG Pub no. US 2001/0042231 A1.

As per claim 1:

Kawamata teaches the semiconductor integrated circuit according to claim 3 comprising: a comparator (paragraph [0029], lines 1-2) comparing a value of data read from each memory cell (paragraph [0029], lines 3-4) connected to an activated word line with an expected value to be read from said each memory cell (paragraph [0029], lines 4-5), for each column in a test mode, an error register accumulatively holding error data based on a comparison result by said comparator (paragraph [0030], lines 1-4), wherein each bit (paragraph [0056], lines 1-2) of said error data indicates said comparison result by said comparator for a corresponding column (paragraph [0039], lines 5-12), and said each bit takes a first logical value when said comparison result for said corresponding column always indicates equality whichever word line is activated, and takes a second logical value when once said comparison result for said corresponding column indicates difference (paragraph [0056], lines 2-6).

As per claim 2:

Kawamata teaches the semiconductor integrated circuit according to claim 1, wherein said semiconductor integrated circuit has a plurality of modules connected to a common internal data bus (Figure 5 # channels D0-D3) and performing reading operations from memory cells simultaneously in the test mode (paragraph [0076], lines 2-12), and said each module includes a switch circuit prohibiting data read from a

memory cell from being output to the internal data bus in the test mode (Figure 9 # S1, paragraph [0076]).

As per claim 3:

Kawamata teaches the semiconductor integrated circuit according to claim 1, wherein said semiconductor integrated circuit has a plurality of modules having their operations controlled by respective chip select signals (Figure 5 # 110, paragraph [0057], lines 1-6), and said each module has a control circuit controlling an operation of reading or writing data from or into a memory cell (claim 3, lines 13-18), irrespective of a value of said chip select signal, in the test mode said plurality of modules receive a common address signal sent through a common internal address bus (paragraph [0059], lines 1-3), where said plurality of modules have word lines different in number, said control circuit in a module that does not have a maximum number of word lines controls an operation of reading or writing data from or to a memory cell (Figure 5 "WEB", (paragraph [0061], lines 1-3), irrespective of a value of said chip select signal, only when values of one or more prescribed bits forming an address signal are prescribed values.

As per claim 4:

Kawamata teaches the semiconductor integrated circuit according to claim 3, wherein said prescribed bits are used in specifying a word line of a module having a maximum number of word lines and are not used in specifying a word line of said module that does not have a maximum number of word lines (paragraph [0061], lines 3-10).

As per claim 6:

Kawamata teaches the semiconductor integrated circuit according to claim 1, wherein said semiconductor integrated circuit has a redundancy circuit in a column (paragraph [0052], lines 1-7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable Kawamata US PG Pub no. US 2001/0042231 A1, and further in view of Urakawa US Patent no. US 6,324,106 B2

As per claim 7-9:

Kawamata substantially teaches a semiconductor integrated circuit comprising: a comparator (paragraph [0029], lines 1-2) comparing a value of data read from each memory cell (paragraph [0029], lines 3-4) connected to an activated word line with an expected value to be read from said each memory cell (paragraph [0029], lines 4-5), for each column in a test mode, an error register accumulatively holding error data based on a comparison result by said comparator (paragraph [0030], lines 1-4), wherein each bit (paragraph [0056], lines 1-2) of said error data indicates said comparison result by said comparator for a corresponding column (paragraph [0039], lines 5-12), and said each bit takes a first logical value when said comparison result for said corresponding column always indicates equality whichever word line is activated, and takes a second logical value when once said comparison result for said corresponding column indicates difference (paragraph [0056], lines 2-6), wherein said semiconductor integrated circuit has a redundancy circuit in a column (paragraph [0052], lines 1-7), and wherein said error register outputs held error data when an address signal indicates a prescribed value (paragraph [0076], lines 1-3)

Kawamata does not explicitly teach a semiconductor integrated circuit wherein said semiconductor integrated circuit further comprising a repair code generation circuit, a program circuit including at least one fuse element for outputting a repair code corresponding to a state of said fuse element, and further elements related to the repair code.

However, Urakawa, in an analogous art, teaches a semiconductor integrated circuit wherein said semiconductor integrated circuit further comprising a repair code

generation circuit receiving said error data for generating a repair code for repairing a defective memory cell array using said redundancy circuit (column 6, lines 10-11), a program circuit including at least one fuse element for outputting a repair code corresponding to a state of said fuse element (column 4, lines 39-41); a register holding a repair code (column 6, lines 8-101); a selector selecting and outputting one of the repair code output from said program circuit and the repair code output from said register (column 10, lines 30-35); and a repair control circuit controlling repair of a defective memory cell array in accordance with the repair code output from said selector (column 6, lines 12-14), and a processor (column 6, lines 54-55) controlling an execution of a two-step test, wherein said processor controls writing of test data into a memory cell (column 5, lines 26-28) and reading of test data from a memory cell without causing said repair control circuit to perform repair in a first step of the test (Figure 7 # 3, column 8, lines 42-44), generates a repair code corresponding to error data stored in said error register in said first step of the test for storage into said register, and controls writing of test data (column 5, lines 26-28) into a memory cell and reading of test data from a memory cell (column 5, lines 28-30) while allowing said selector to output the repair code from said register to cause said repair control circuit to perform the repair. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the fuse element and repair code circuitry to memory testing apparatus of Kawamata. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that applying the fuse would have allowed to shift the comparator

result to adjoining memory cell column without using a memory cell column in which the defective cell exists, and repair code circuitry would have allowed for the recovery of the defective bit.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to the final action is set to expire in THREE MONTH from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of the final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Saqib Siddiqui
Art Unit 2138
07/08/2006

GUY LAMARRE
PRIMARY EXAMINER